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Approved for use in integrated circuit layout design under 35 U.S.C. 154.

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Sheet 1 of 1

<b>Complete if Known</b>	
Application Number	10/578,550
Filing Date	July 6, 2007
First Named Inventor	Brian Ruby
Art Unit	1715
Examiner Name	Joseph Albert Miller, Jr.
Attorney Docket Number	09-1540

## U. S. PATENT DOCUMENTS

## FOREIGN PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T <sup>6</sup>
		Country Code <sup>3</sup> -Number <sup>4</sup> -Kind Code <sup>5</sup> (if known)				
		JP-2002-206169	07-26-2002	Seiichi, Suenaga et al.	15,22,29,47-56,60-63, Fig. 2	
		JP-2003-12313	08-04-2004	Sato, Hironori et al.	19	
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